	Тур	e L	# Hits	Search Text	DBs	Time Stamp	o m m	ef	Er ro rs
1	BRS	S L15	150	(ammonia or NH3) and (CF4 or C4F8 or C4F6 or C5F8 or C2F6 or C3F8 or CHF3 or CH2F2)	USPAT; US-PGPUE EPO; JPO; DERWENT IBM_TDB	3; 2003/01/18 20:06			0
2	BRS	L22	110	15 and @pd<=20001210	USPAT; US-PGPUB EPO; JPO; DERWENT IBM_TDB	[;] 2003/01/18 20:18			0
3	BRS	L29	0	22 and 252/\$ccls.	USPAT; US-PGPUB EPO; JPO; DERWENT; IBM_TDB	, 2003/01/18 20:07			0
4	BRS	L36	1	22 and 252/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/01/18 20:08)
5	BRS	L43	22	22 and 438/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/01/18 20:17		C)
6	BRS	L50	9	(CF4 with CHF3 with CH2F2) with etch\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/01/18 20:18		0	
7	BRS	L57	6	50 and @pd<=20001210	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/01/18 20:23		0	
8	BRS	L64	88		USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/01/18 20:23		0	

CLIPPEDIMAGE= JP02000294537A

PAT-NO: JP02000294537A

DOCUMENT-IDENTIFIER: JP 2000294537 A

TITLE: ETCHING DEVICE AND METHOD THEREFOR

PUBN-DATE: October 20, 2000

INVENTOR-INFORMATION:

NAME COUNTRY ODA, TAKUJI N/A MATSUO, HIROSHI N/A YOKOYAMA, YUICHI N/A MAEDA, SEIJI N/A YAMAMOTO, YUJI N/A NAKAJIMA, YOSHIYUKI N/A INOUE, SHINYA N/A

ASSIGNEE-INFORMATION:

NAME COUNTRY

MITSUBISHI ELECTRIC CORP N/A

RYODEN SEMICONDUCTOR SYST ENG CORP N/A

APPL-NO: JP11099894

APPL-DATE: April 7, 1999

INT-CL (IPC): H01L021/3065; C23F004/00

ABSTRACT:

PROBLEM TO BE SOLVED: To provide an etching device and method for obtaining the

sidewall of a silicon nitride film, having film thickness and height sufficient for electrical insulation at the sidewall part of a pattern having a step in level.

SOLUTION: A silicon nitride film 5 is <u>etched</u> by using the plasma of a mixed gas, containing at least one of <u>CF4 and CHF3 and CH2F2</u> in a discharge

chamber

separation type dry <u>etching</u> device, so that a sidewall 7 of a silicon nitride film 5 can be left on the widewall of a pattern to be self-aligned, and the silicon nitride film 5 at the bottom part of the pattern can be removed. Also, the silicon nitride film 5 of a memory cell part is removed, and simultaneously the silicon layer and metallic silicide layer or the like of a peripheral circuit part in the same substrate surface as the memory cell part are etched also.

COPYRIGHT: (C)2000,JPO